REMARKS

This amendment is being filed in response to the Office Action having a mailing date of September 20, 2005. Claims 1-7 are amended as shown. New claims 8-16 are added. No new matter has been added. With this amendment, claims 1-16 are pending in the application.

I. Priority Application

In the Office Action, the Examiner acknowledged the applicants' claim to foreign priority, but indicated that the applicant has not filed a certified copy of the priority application (EP Application Serial No. 00830735.7, filed on November 7, 2000). The applicants respectfully note that a certified copy of the priority application was in fact filed on March 22, 2002.

Indeed in the U.S. Patent Office PAIR system, the Image File Wrapper of the present application shows a hyperlink dated March 22, 2002 that is labeled as "Artifact sheet indicating an item has been filed which cannot be scanned" (emphasis added). Upon further examination of the hyperlinked document in PAIR, it appears that the "item" was not scanned because it was a "bound document." The applicants believe that this un-scanned "item" was the certified copy of the priority application, since the certified copy was a bound document. Thus, the certified copy appears to have been properly received and entered in the file by the U.S. Patent Office.

The applicants respectfully request the Examiner to double check the file of the present application to confirm whether or not the previously filed certified copy of the priority document is present therein. If the certified copy of the priority document is not present therein, then the Examiner is kindly requested to inform the applicants in the next communication whether or not the Examiner wishes the applicants to submit a replacement certified copy of the priority document.

II. Information Disclosure Statement

In the Office Action, the Examiner stated that the Information Disclosure Statement (IDS) of November 7, 2001 fails to comply with requirements. The applicants

respectfully disagree with this conclusion by the Examiner, and also note that the IDS was in fact filed on March 22, 2002 (rather than on November 7, 2001 as indicated by the Examiner). Copies of both listed references were submitted with the IDS, and indeed PAIR shows a scanned copy of at least one of the references (*i.e.*, the foreign patent document GB 2318664A). Moreover, both references (including the foreign patent document) are in the requisite English language. Thus, all requirements for having theses references entered and considered by the Examiner have been sufficiently met by the applicants.

Accordingly, the applicants kindly request the Examiner to consider and confirm in the next communication that the information in the previously filed references/IDS has been considered. If the Examiner believes that the IDS is still non-compliant, then the Examiner is kindly requested to specifically point out the manner in which the IDS is non-compliant, so that the applicants can appropriately address the issue.

III. Discussion of the Applicants' Embodiments in View of the Cited References

In the Office Action, claims 1-7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Allen (U.S. Patent No. 6,151,568). For the reasons set forth below, the applicants respectfully request the Examiner to reconsider, and to allow all of the pending claims.

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

As described in the present application, an embodiment provides a method to estimate power consumption, over a given time interval, of a digital circuit described at a level of a functional element provided with input/output terminals. The digital circuit may for example be cell G generically shown in Figure 1, described at a hardware abstraction level (in this example, at the gate level).

An additional element B is provided, such as shown in Figure 2, that is associated to the cell G. The element B is also at some hardware abstraction level, such as at a gate or RTL level corresponding to the cell G.

According to one example embodiment, the information used for power consumption estimation includes: a) a time interval in which the estimation is to be made; b) the number of transitions performed during the time interval; and c) the fraction of time in which the state is stable within the time interval. In one of the disclosed embodiments, the additional element B is able to perform operations to obtain b) and c). *See, e.g.*, page 6, lines 17 of the present application.

In contrast, the prior art uses simulation techniques that involve extraction of the switching activity of the circuit, in conjunction with estimation of power consumption via dedicated software, starting with the extracted switching activity. *See, e.g.*, page 3, lines 1-5 of the present application.

Allen, which was cited by the Examiner in the present Office Action, represents the general prior art described above. Allen acquires determines toggle/switching rates, and then uses this information to estimate the power consumption. *See, e.g.*, column 10, lines 31-38 of Allen.

Allen does not disclose, teach, or suggest emulation at the hardware level corresponding to an abstraction level of the digital circuit, such as the gate level or at the RTL level. Indeed, the very title of Allen is "Power Estimation Software System" (emphasis added), which clearly indicates that Allen is not performing power consumption estimation based on emulation at some hardware abstraction level, but is rather using software simulation techniques similar to the known prior art. It is further clear that Allen does not further provide any sort of "additional element" (such as the element B) at all, at a hardware abstraction level, to perform power estimation.

Moreover, Allen does not disclose, teach, or suggest detection of the number of transitions performed by the functional element (such as the element G) during the time interval. Column 10, lines 31-38 merely talk about the calculation of the toggle rate by counting the

number of transitions over a general period of time, and does not tie or otherwise specifically relate the number of transitions to a given time interval during which power consumption occurs.

The Examiner has also cited Allen's use of duty cycles to determine power consumption. However, the duty cycles described on column 10, lines 38-40 of Allen is merely described as the percentage of time in which a signal is in an active state. Again, there is nothing that ties Allen's duty cycle to a specific given time interval (*e.g.*, power consumption during the given time interval). Allen simply provides a percentage, which can occur at any indefinite time period.

Raman (U.S. Patent No. 5,535,370), which was submitted by the applicants in the previous IDS, does not cure the deficiencies of Allen. Raman discloses simulation techniques similar to the known prior art simulation techniques for power consumption estimation discussed above.

IV. Discussion of the Claims

Claim 1 has been amended to recite emulating --at a hardware level corresponding to an abstraction level of the digital circuit--. As explained above, Allen does not provide this feature. Allen simply provides a software simulation technique, and does not emulate at a hardware abstraction level.

On page 3 (paragraph 4) of the present Office Action, the Examiner interpreted the statement "emulating at the hardware level" to mean "running a simulation on any hardware peripheral." With the amendment to claim 1 discussed above, the emulation at the hardware level of claim 1 now clearly distinguishes over the software simulation of Allen and/or distinguishes over the interpretation made by the Examiner, and is now allowable.

Claim 1 recites the "additional elements." As explained above, Allen does not disclose, teach, or suggest such additional elements, particularly additional elements emulated at a hardware level corresponding to an abstraction level of the digital circuit. Allen merely uses computer software to run the simulation. Thus, claim 1 is further allowable over Allen.

Claim 1 is further amended to recite --estimating the power consumption based on a number of transitions performed by the simulated functional element during said time

interval--. Again as explained above, this feature is not disclosed, taught, or suggested by Allen. That is, Allen simply determines a toggle rate, and this toggle rate is not related to any given time interval over which power consumption occurs. Therefore, claim 1 is further allowable over Allen.

Dependent claim 5 recites that the additional emulated element is "able to detect, during said given time interval: a fraction of time in which a state of the associated functional element is stable" and further recites that "the value of the number the value of said number of transitions and said fraction of time being indicative of the power consumption of said functional element during said time interval." Again, these features are not disclosed, taught, or suggested by Allen. Allen merely detects the duty cycle, and does not provide any specific relationships between the duty cycle and any given time interval in which power consumption occurs (and is estimated). Accordingly, dependent claim 5 is allowable.

New dependent claims 8 and 9 specify that the hardware levels include the RTL level and the gate level, respectively. Since Allen performs software simulation, and does not emulate at these or other hardware abstraction levels using an additional element, dependent claims 8 and 9 are clearly allowable.

New independent claim 10 recites features that are distinctive over Allen and the other references, whether singly or in combination. For example, means for emulating at a hardware abstraction level is recited, along with means for estimating the power consumption based on the acquired number of transitions performed by the simulated functional element during the time interval. Therefore, claim 10 is allowable.

Dependent claims 11-12 recite distinctive features along the lines of those previously discussed above, such as RTL/gate abstraction levels, a stable state during the time interval, and so forth. These dependent claims 11-12 are allowable.

New independent claim 13 similarly recites features allowable over Allen or the other references, whether singly or in combination, including a feature to emulate at a hardware abstraction level. Dependent claims 14-16 also recite distinctive subject matter, and are allowable.

V. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

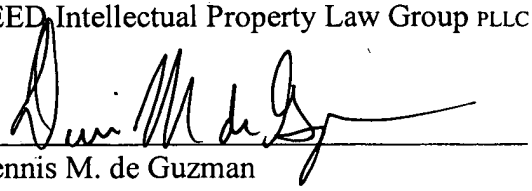
If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



Dennis M. de Guzman
Registration No. 41,702

DMD:wt

Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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